This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-19 (canceled).

20. (currently amended) A system comprising:
a bus;
a plurality of bus masters each having real-time requirements for mastership of the bus; ~~and~~
an arbiter ~~including means~~ for allocating bus mastership to ~~a given~~ the bus masters, the arbiter being arranged so that the amount of time that each bus master can gain bus access is ~~as~~ a percentage of the total bus time, and
prioritization means for allocating priority levels for bus mastership when a given bus master does not request bus mastership during its allocated percentage of time.

21. (canceled).

22. (currently amended) A Queue Management System (QMS) ~~system~~ supporting a plurality of queue users using a bus, each queue user being a bus master having real-time requirements for mastership of the bus, said QMS system comprising:

an arbiter ~~including means~~ for allocating mastership of the bus to a given bus master, said mastership allocated as a percentage of the total bus time; and

means for allocating priority levels for bus mastership when the given bus does not require bus mastership during its allocated percentage of the total bus time.

Claim 23 (canceled).

24. (currently amended) The QMS system according to claim 22 ~~23~~, further comprising a queue portal for each of the queue users, a respective queue user interface being positioned between each queue user and its corresponding queue portal.

25. (previously presented) The QMS system according to claim 24, said QMS further comprising a memory for storing data as said data passes through said QMS; wherein one of the queue users is a processor.

26. (previously presented) The QMS system according to claim 25, said arbiter further including a state machine for allocating to each bus master its percentage of the total bus time.

27. (previously presented) The QMS system according to claim 26, wherein said state machine determines an active queue portal arbitration by cycling through a predetermined

number of states, in a fixed order or every clock cycle, each of said states being associated with a respective queue portal.

28. (previously presented) The QMS system according to claim 27, wherein said percentage of total bus time allocated to a given queue user is determined by a total number of states associated with a given queue portal corresponding to said given queue user.

29. (previously presented) The QMS system according to claim 28, wherein, when a given state is active and the given queue user corresponding to said given queue portal associated with said given state does not request bus mastership, then said means for allocating priority levels for bus mastership is activated.

30. (previously presented) The QMS system according to claim 29, wherein said arbiter allocates the highest priority level to bus accesses by a non-interruptible memory sequence triggered by the processor.

31. (previously presented) The QMS system according to claim 30, wherein said arbiter allocates a second highest priority level to bus accesses by the processor.

32. (currently amended) The QMS system according to claim 31 ~~32~~, wherein said arbiter allocates a third highest priority level to bus accesses by said QMS.

33. (previously presented) The QMS system according to claim 23, said arbiter further including a state machine for allocating to each bus master its percentage of the total bus time.

34. (previously presented) The QMS system according to claim 33, wherein said state machine determines an active queue portal arbitration by cycling through a predetermined number of states, in a fixed order or every clock cycle, each of said states being associated with a respective queue user.

35. (previously presented) The QMS system according to claim 34, wherein said percentage of total bus time allocated to a given queue user is determined by a total number of states associated with the given queue user.

36. (previously presented) The QMS system according to claim 35, wherein, when a given state is active and the given queue user associated with said given state does not request bus mastership, then said means for allocating priority levels for bus mastership is activated.

37. (currently amended) A Queue Management System (QMS) ~~system~~ supporting a plurality of queue users using a bus, each queue user being a bus master having requirements for mastership of the bus, said QMS system comprising:

a plurality of queue portals, each queue user being associated with a corresponding queue portal; and

an arbiter including:

means for allocating bus mastership to a given queue user as a percentage of total bus time, said means for allocating bus mastership having a state machine,

wherein said state machine cycles through a predetermined number of states, each of said states being associated with a corresponding queue portal and thus also being associated with a corresponding queue user associated with said corresponding queue portal, and further

wherein, when a given state is active, the corresponding queue user associated with said corresponding queue portal associated with said given state is allocated bus mastership, and still further

wherein said percentage of total bus time allocated to said given queue user is determined by the total number of states associated therewith as compared to the total number of states; and

means for allocating priority levels for bus mastership which is activated when the queue user associated with a specific state does not request bus mastership when said specific state is active.

38. (previously presented) A Bluetooth baseband peripheral comprising:

a QMS system according to one of claims 22-37;

a re-usable microprocessor block;

link control hardware for communication with Bluetooth devices via a radio IC and a QMS system; and

an interface block between the bus and said re-usable microprocessor block,

the queue users comprising:

a communication control block;

a host queue user;

a voice encoder/decoder; and

a processor forming part of said re-usable microprocessor block,

wherein each of said queue users is connected to the bus via its queue user interface and a respective bus master and bus tri-state driver.

39. (previously presented) A Bluetooth baseband peripheral comprising:

a QMS system according to one of claims 22, 23, 28, 29, 32, 35, 36, and 37;

a re-usable microprocessor block;

link control hardware for communication with Bluetooth devices via a radio IC and a QMS system; and

an interface block between the bus and said re-usable microprocessor block.

40. (currently amended) ~~The Bluetooth baseband peripheral according to claim 39, wherein the queue users is one or more of a communication control block, a host queue user,~~

~~40. (new)~~ The Bluetooth baseband peripheral according to claim 39, wherein the queue users is one or more of a communication control block, a host queue user, a voice encoder/decoder, and a processor forming part of said re-usable microprocessor block, and further

wherein each of said queue users is connected to the bus via its queue user interface and a respective bus master and bus tri-state driver.

41. (previously presented) A Bluetooth baseband peripheral comprising:

a QMS system according to one of claims 22, 23, 29, 36, and 37; and

link control hardware for communication with Bluetooth devices via a radio IC and a QMS system.